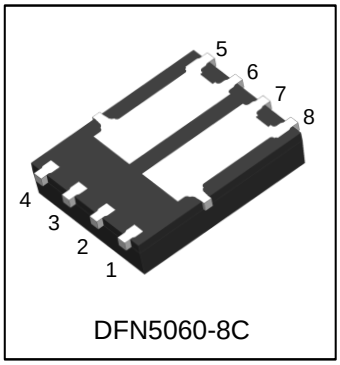
S-LDN7407HZDT3WG

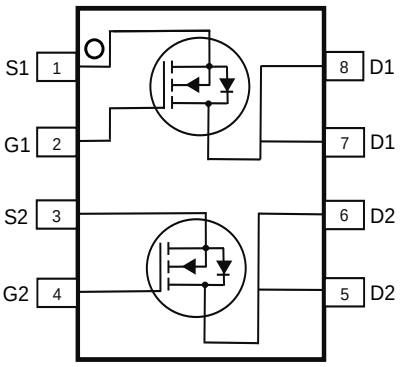
40V N-Channel Power Dual MOSFET



DFN5060-8C

1. FEATURES

- RDS(on)≤7mΩ@VGS=10V.
- Low thermal impedance.
- Fast switching.
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S- prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.



2. APPLICATIONS

- Power Tools
- DC/DC conversion
- Motor Control

3. DEVICE MARKING AND RESISTOR VALUES

Device	Marking	Shipping
S-LDN7407HZDT3WG	LDN7407HZ	5000/Tape&Reel

4. MAXIMUM RATINGS

Parameter		Symbol	Limits	Unit
Drain-to-Source Voltage		VDS	40	V
Gate-to-Source Voltage		VGS	± 20	V
Continuous Drain Current(Note 1)	TA=25℃	ID	15	A
	TA=100℃		11	
Pulsed Drain Current (Note 2)	TA=25℃	IDM	60	
Continuous Drain Current	TC=25℃	ID	85	A
	TC=100℃		60	
Pulsed Drain Current	TC=25℃	IDM	340	
Avalanche Current		IAS	23	A
Avalanche Energy(L=0.1mH)		EAS	26	mJ
Power Dissipation(Note 1)	TA=25℃	PD	2.3	W
	TA=100℃		1.2	
Power Dissipation	TC=25℃	PD	75	W
	TC=100℃		37.5	
Operating Junction and Storage Temperature Range		TJ/TSTG	-55~+175	℃

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance,Junction-to-Ambient(Note 1)	RθJA	65	℃/W
Thermal Resistance,Junction-to-Case	RθJC	2	

Note:1.Surface mounted on "1.5in x 1.5in" FR4 board using 1*1 in pad, 2 oz Cu.

2.Pulse width limited by maximum junction temperature.

6. ELECTRICAL CHARACTERISTICS(TJ=25℃ unless otherwise specified)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Static						
Drain to Source Breakdown Voltage (VGS = 0 V, ID = 250 μA)		BVDSS	40	-	-	V
Gate-Source Threshold Voltage (VDS = VGS , ID = 250 uA)		VGS(th)	2	3	4	V
Gate-Body Leakage (VDS = 0 V, VGS = ±20 V)		IGSS	-	-	± 100	nA
Zero Gate Voltage Drain Current (VDS = 40 V, VGS = 0 V)		IDSS	-	-	1	μA
Drain-Source On-Resistance(Note 3) (VGS = 10 V, ID = 20 A)		RDS(on)	-	5.5	7	mΩ
Transconductance (VDS = 5 V, ID = 20 A)		gfs	-	71	-	S
Dynamic						
Input Capacitance	(VDS = 20 V, VGS = 0 V, f = 100kHz)	Ciss	-	950	-	pF
Output Capacitance		Coss	-	513	-	
Reverse Transfer Capacitance		Crss	-	15	-	
Total Gate Charge	(VDS = 20 V, VGS = 10 V,ID = 20 A)	Qg	-	14.3	-	nC
Gate-Source Charge		Qgs	-	5	-	
Gate-Drain Charge		Qgd	-	3.2	-	
Turn-On Delay Time	(VDS = 20 V, ID = 20 A, VGEN = 10 V, RG = 3 Ω)	td(on)	-	11	-	ns
Rise Time		tr	-	11	-	
Turn-Off Delay Time		td(off)	-	23	-	
Fall Time		tf	-	10	-	
Gate Resistance (VDS = 0 V,VGS = 0 V,f = 1.0MHz)		Rg	-	5.5	-	Ω
Diode characteristics						
Diode Continuous Current TC = 25℃		IS	-	-	75	A
Diode Plused Current TC = 25℃		ISM	-	-	300	A
Diode Forward Voltage (IS = 20 A,VGS = 0 V)		VSD	-	0.8	1.2	V
Reverse Recovery Time (VR=20V,IF=20A,dIF/dt=100A/us)		trr	-	60	-	ns
Reverse Recovery Charge (VR=20V,IF=20A,dIF/dt=100A/us)		Qrr	-	63	-	nC

3.Pulse test: PW ≤ 300us duty cycle ≤ 2%.

7. ELECTRICAL CHARACTERISTICS CURVES

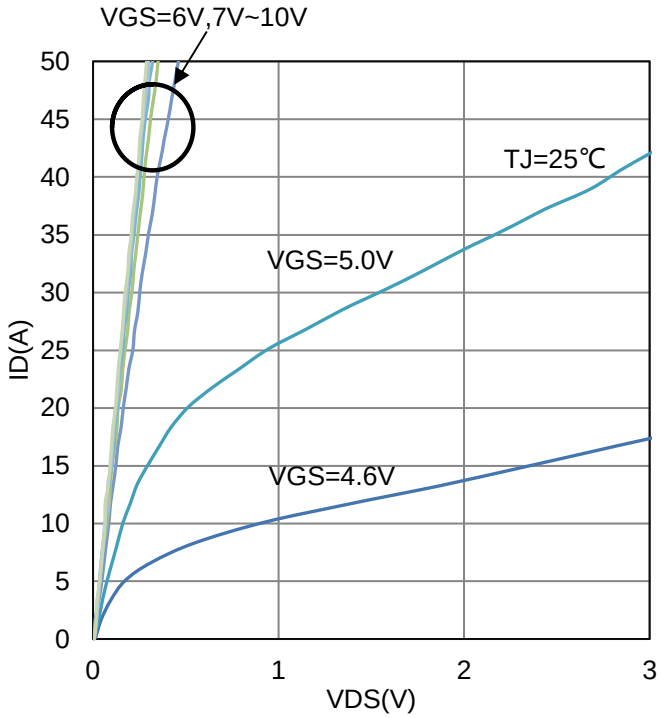


Figure 1.ID vs. VDS

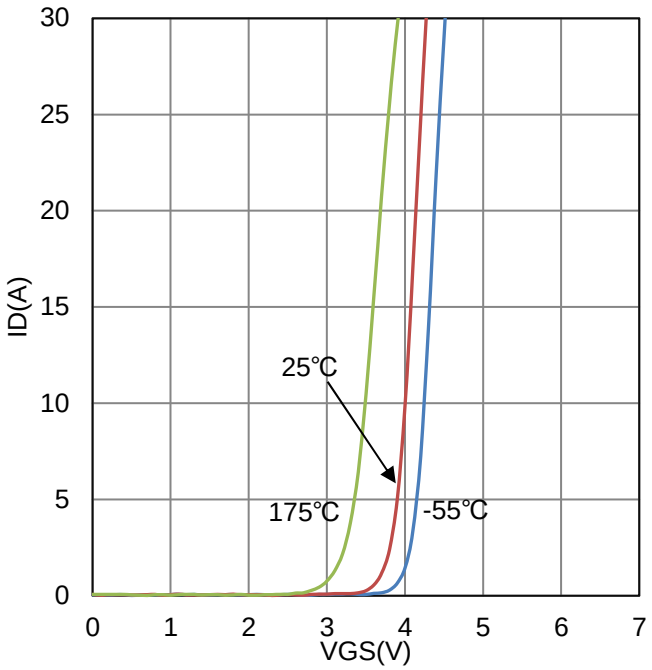


Figure 2.ID vs. VGS

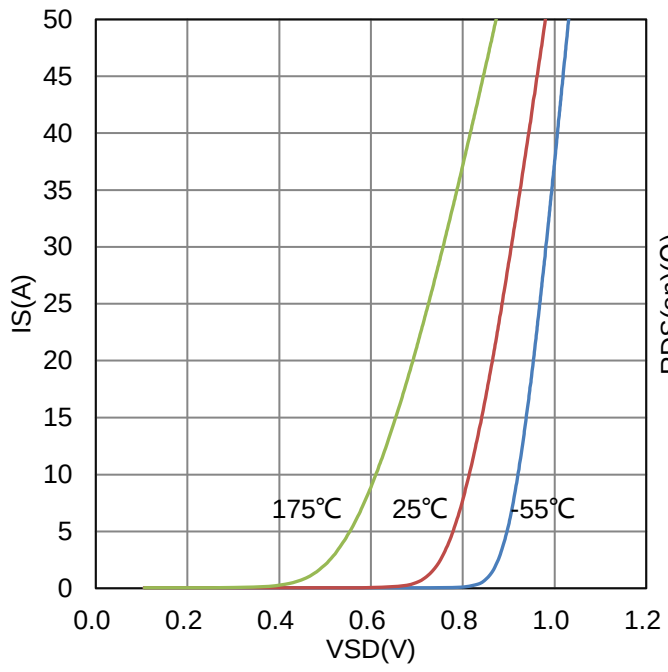


Figure 3.IS vs. VSD

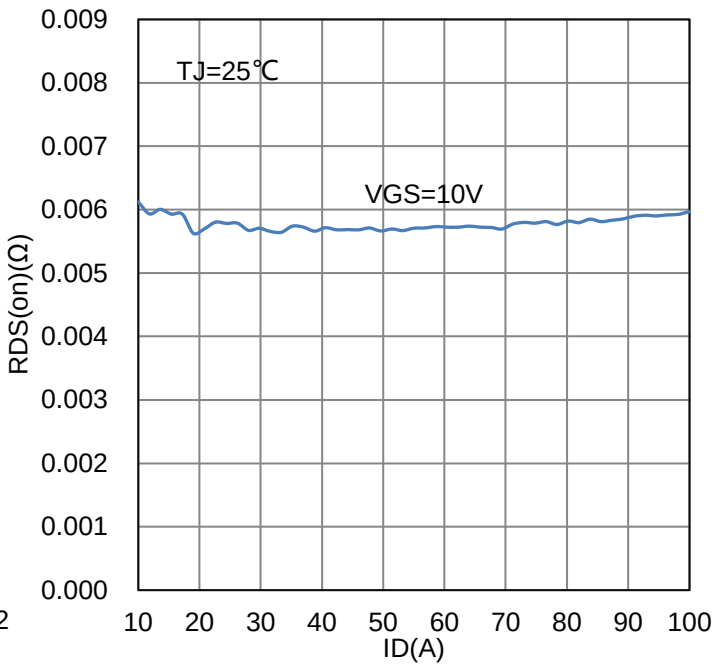


Figure 4.RDS(on) vs. ID

7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

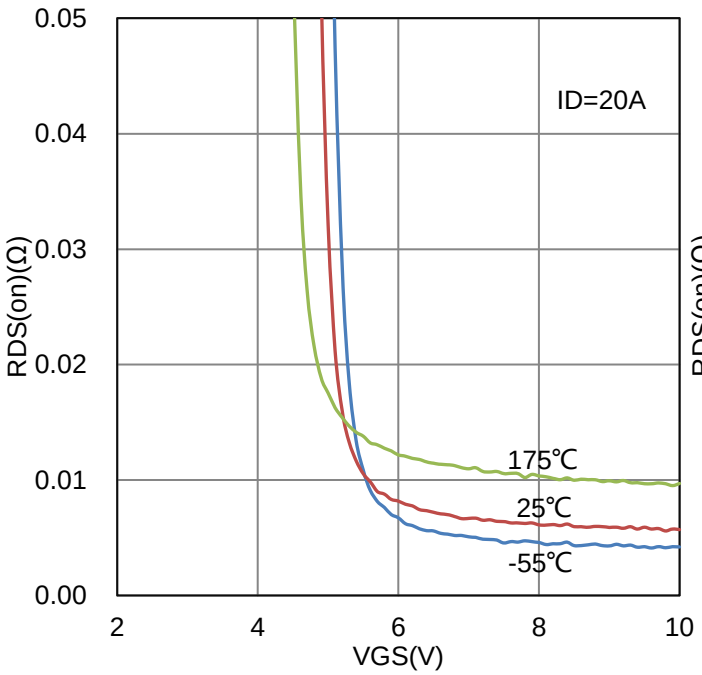


Figure 5.RDS(on) vs. VGS

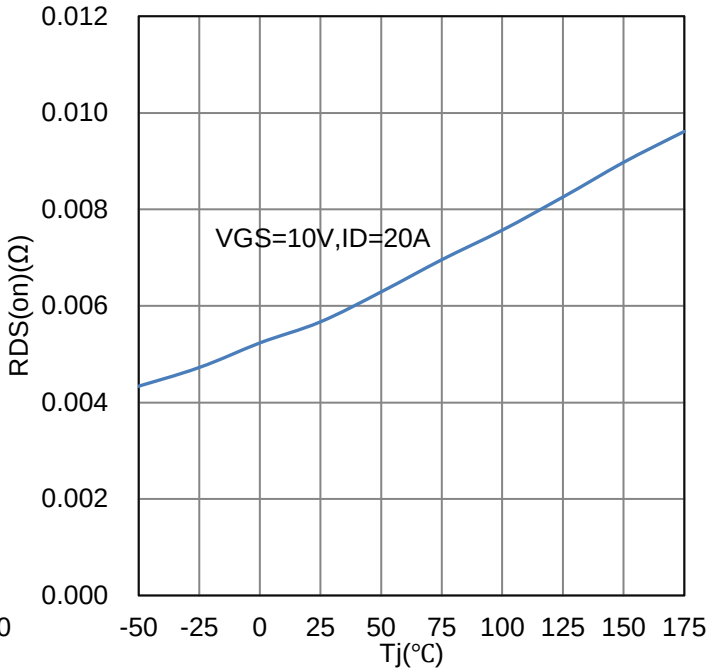


Figure 6.RDS(on) vs. Tj

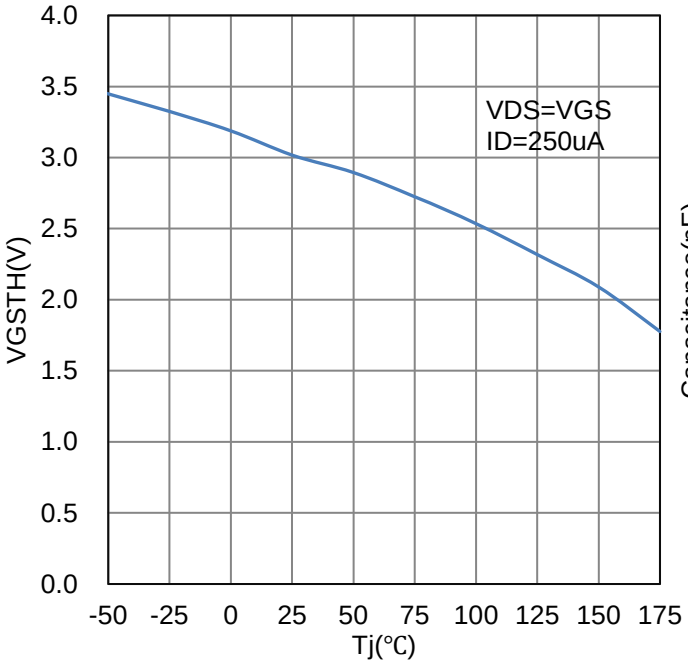


Figure 7.VGSth vs. Tj

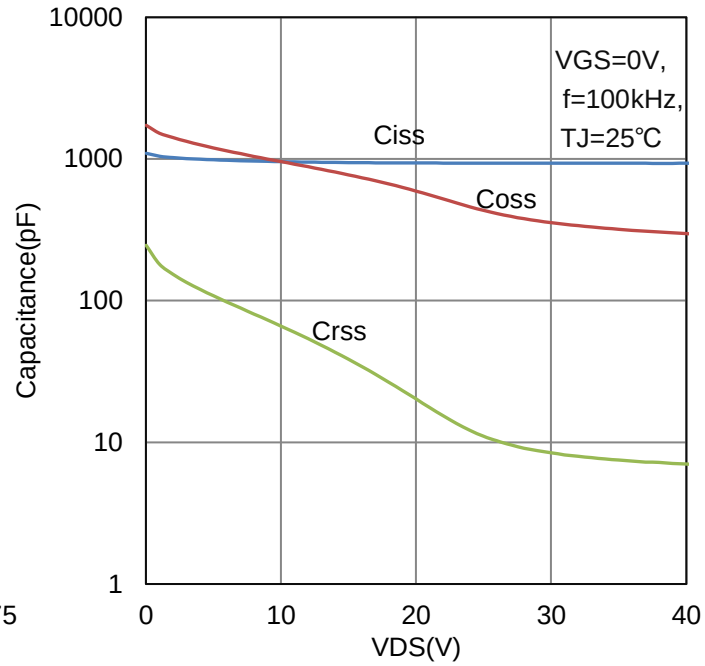


Figure 8.Capacitance

7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

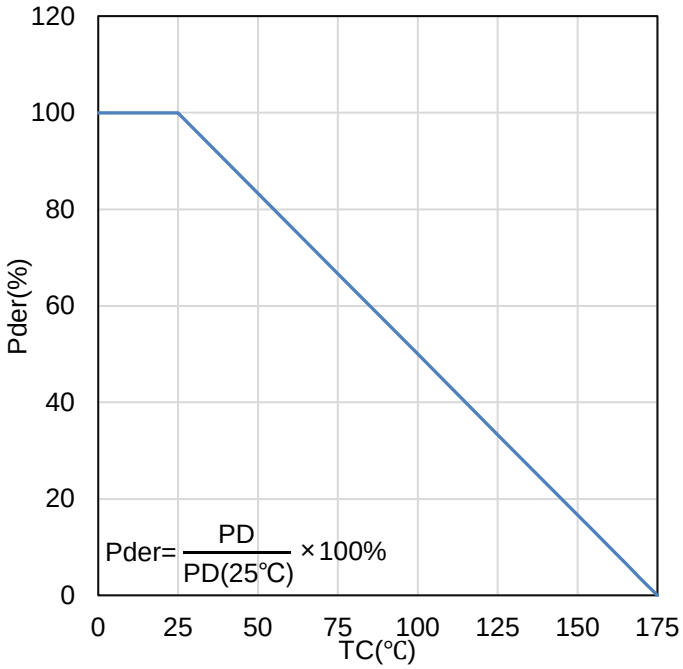


Figure 9.Normalized Derating Curve

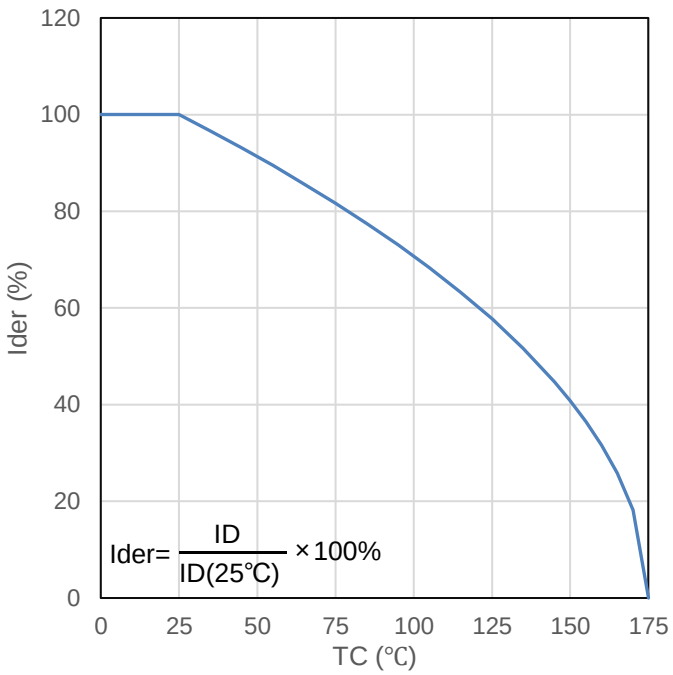


Figure 10.Normalized drain Current

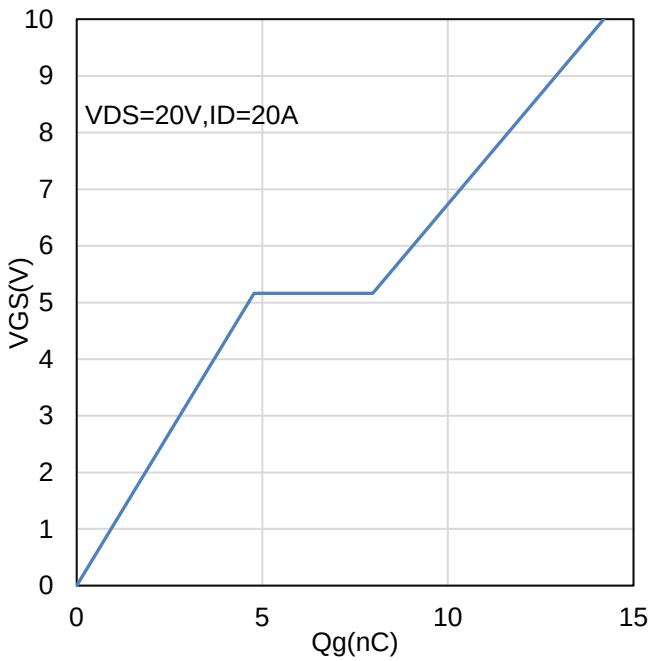


Figure 11.VGS vs. Qg

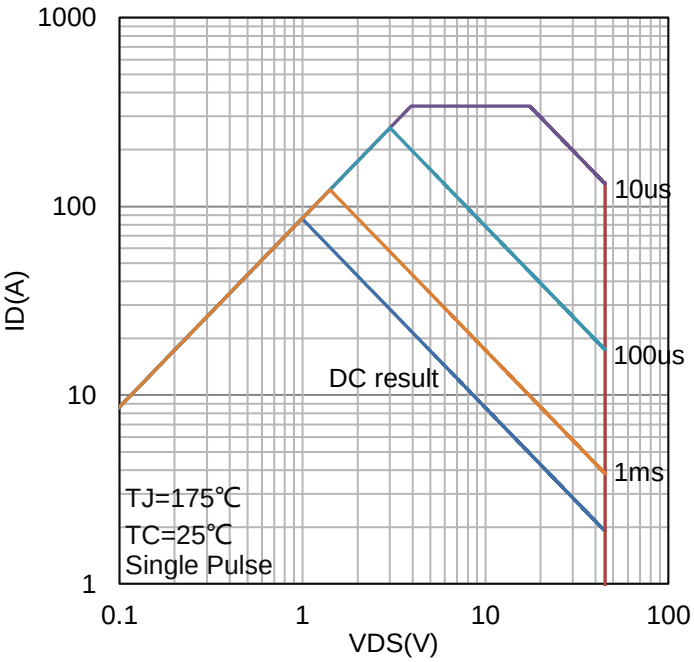


Figure 12.Safe Operating Area

7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

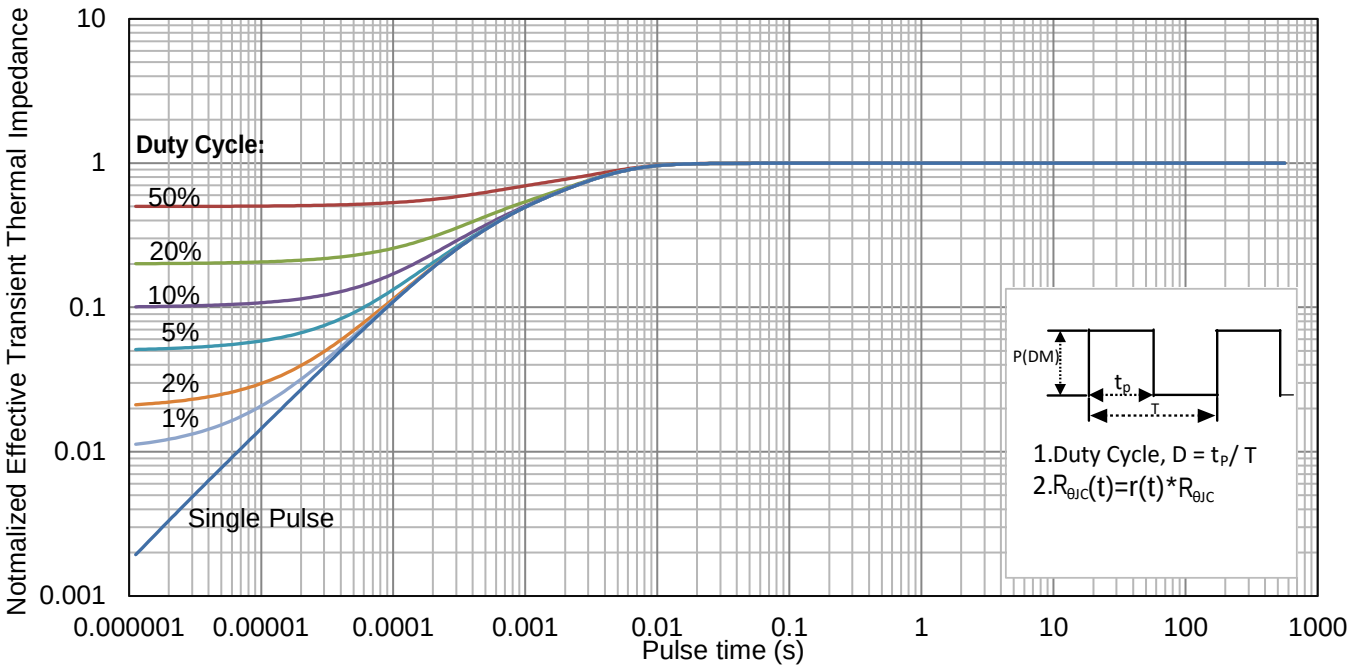
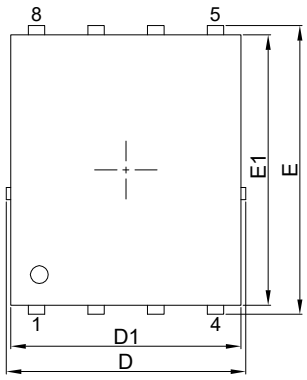


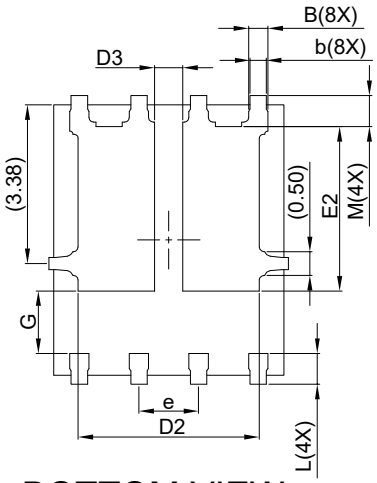
Figure 13.Thermal Response

8.OUTLINE AND DIMENSIONS

DFN5060-8C(T1.00)

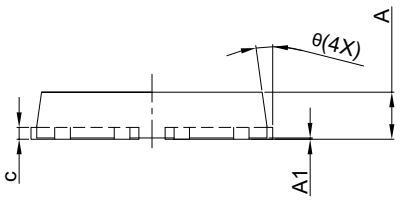


TOP VIEW



BOTTOM VIEW

symbol	dimensions in mm		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	—	0.05
B	0.36	0.41	0.46
b	0.30	0.35	0.40
c	0.254 REF		
D	4.95	5.10	5.25
D1	4.80	4.90	5.00
D2	3.76	3.86	3.96
D3	0.55	0.60	0.65
E	6.00	6.15	6.30
EI	5.66	5.76	5.86
E2	3.40	3.50	3.60
G	1.34 BSC		
e	1.27 BSC		
L	0.56	0.66	0.76
M	0.56	0.66	0.76
θ	0°	—	12°

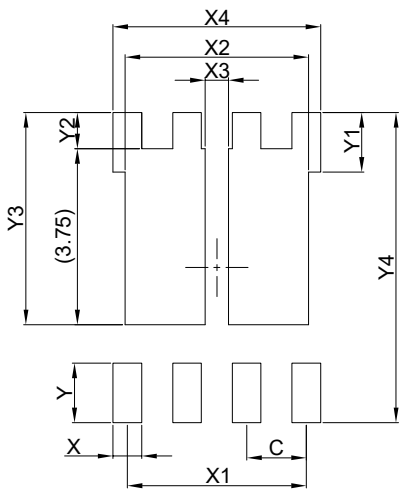


SIDE VIEW

GENERAL NOTES

1. Top package surface finish Ra Max0.4um
2. Bottom package surface finish Ra Max0.4um
3. Side package surface finish Ra Max0.4um
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side.
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

9.SOLDERING FOOTPRINT



DFN5060-8C	
DIM	(mm)
C	1.27
X	0.61
X1	3.81
X2	3.91
X3	0.50
X4	4.42
Y	1.27
Y1	1.27
Y2	0.77
Y3	4.52
Y4	6.61

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.

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